Tuning Verilog-A PSP Model to a Specific Technology

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Abstract –**The method of tuning a Verilog-A PSP model to a specific technology is presented in this paper. The mechanisms of defining the required model parameters, their extraction, and the implementation of the respective changes in Verilog-A are described. New program tool for extraction (Extract CAD) is utilized together with CADENCE Spectre simulator for the circuit simulations of the Verilog-A code.**

Keywords – **PSP model, Verilog-A, CADENCE, Extract CAD, parameter extraction, simulation.**

I. INTRODUCTION

PSP Model

Modeling is at the core of any design process. Compact MOSFET models are an essential bridge between the fabrication process development and the circuit design. Their primary function is to accurately reproduce the device characteristics in details, which are essential to the design of digital, analog, mixed-signal, and RF integrated circuits. There is a wide consensus in the compact modeling community that traditional threshold-voltage-based models of MOSFETs need to be replaced with the more advanced surface-potential-based or inversion-charge- based models [1]). One of the motivations for choosing the surface-potential-based approach is that it enables the physical modeling of the device. Despite the clear physics and the ability to provide a single expression for all regions of operation [2] surface-potential-based models did not become popular until the last decade due, in part, to their perceived complexity. Successful surface-potential-based models became possible only after significant progress was made in the techniques for the computing the surface potential, simplification of the charge equations and the introduction of small-geometry effects. The implementation of these advances and the overall model structures of SP [3] and MM11 [4] turned out to be compatible, enabling the merger of both models into a single new model called PSP that combines the features of SP and MM11.

The major features of PSP include: physical surface-potential-based formulation in both intrinsic and extrinsic model modules, physical and accurate description of the accumulation region, inclusion of all relevant small geometry effects, modeling of the halo implant effects, including the output conductance degradation in long devices, Coulomb scattering and non-universality in the mobility model, non-singular velocity-field relation enabling the modeling of RF distortions including intermodulation effects (IM3), complete Gummel symmetry, mid-point bias linearization enabling accurate modeling of the ratio-based circuits (e.g. R2R circuits), quantum-mechanical corrections, correction for the polysilicon depletion effects, GIDL/GISL model, surface-potential-based noise model including channel thermal noise, flicker noise and channel-induced gate noise, advanced junction model including trap-assisted tunneling, band-to-band tunneling and avalanche breakdown, spline-collocation-based NQS model including all terminal currents, stress model [1].

The model structure consists of a core and enhancement blocks. The core block contains the quasi-static (QS) intrinsic and the extrinsic models. The intrinsic model contains expressions for the drain current, terminal charges and the noise sources. The extrinsic model includes contributions of the source-drain overlap regions, gate and substrate currents, etc. The enhancement block contains junction model developed using the NQS module [5, 6].

PSP distinguish between local and global model parameters. Global parameters include geometry dependences and before evaluating MOSFET output characteristics are converted into a small number (about 35) of local parameters actually used in the core model. The actual local parameters used in circuit simulations are then recomputed from the global parameters.

Verilog-A

Verilog-A is the analog extension to the Verilog hardware description language. It provides the ability to describe analog functions of electronic circuits behaviorally by means of mathematical equations, or conditional signal assignments. The use of Verilog-A for implementation of sophisticated models speeds up the design time and simulation process. Verilog-A is embedded in CADENCE Specter simulator which makes it easy to create and include custom model cells.

This paper focuses on the method of implementation of the DC core of the PSP compact model in Cadence Design Systems using Verilog-A HDL. The procedure for parameter extraction from standard CMOS technology is presented and the respective implementation of these

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parameters to the PSP model card is given. Extract CAD tool is used for the extraction process.

II. MODEL ADAPTATION AND PARAMETERS EXTRACTION

The Verilog-A PSP model gives a general pattern for transistor parameters. The use of HDL-AMS provides the ability to easily tune up model parameters for a specific technology. For this reason the model parameter values are required.

Verilog-A PSP code is supported by Arizona State University and NXP Semiconductors [8]. Since its code is open it allows the flexibility of custom applications. One option is to take the free code from the developer site and to implement as individual library cell; this cell can afterwards be treated as global cell that is parameterized with specific parameters for each instance. The other option is to modify the free code hardcoding the parameters of a given technology; thus each instance complies with the parameter set of the chosen technology and is applicable for designs with this particular technology only.

A part of this research aims to obtain a set of *local parameters* for a particular NMOS device from a given technology. Once this set is obtained the PSP Verilog-A code is edited and compiled in Cadence Analog Environment in order to produce simulation data.

In this paper the Extract CAD software is used [9]. The Extract CAD software allows receiving the model card with local parameters for a specific device based on the input technology parameters and simulation data. This tool provides the ability to extract and tune up the local PSP model parameters. This program requires minimal number of process parameters, needed to define basic characteristics of the technology used. The values of the process parameters that are not explicitly given in the technology specifications are calculated by appropriate techniques. Both parameters are given in Table 1. In this research the AMS CMOS 0.35 technology along with CADENCE simulation environment is used.

TABLE 1. CALCULATED PROCESS PARAMETERS

Name	Unit	Calculated	Min	Max	Description
	Process Parameters				
VFB	V	-1	-	-	Flat-band voltage at TR
TOX	m	$7{,}6\ 10^{-9}$	10^{-10}	-	Gate oxide thickness
NEFF	m^{-3}	$2{,}12.10^{23}$	10^{20}	10^{26}	Substrate doping
NP	m^{-3}	727	0	-	Gate poly-silicon doping
TOXOV	m	$7{,}6\ 10^{-9}$	10^{-10}	-	Overlap oxide thickness

Other data required by the Extract CAD tool is that provided by the DC characteristics of the transistor with specific instance parameters. As this kind of information is not directly given it was provided by means of device simulations in CADENCE simulation environment.

Parameters extraction

Process parameter values given in Table 1 are taken from the technology process data where available. Those that are not directly defined are obtained by calculations and simulation indirectly.

The parameter V_{FB} is obtained with simulations according to the method proposed by Dieter K. Schroder in [7], by tracing the C-V characteristic of the transistor. The required value of V_{FB} is equal to the value of the gate voltage at a specific point of the curve.

The poly-silicon gate doping NP is calculated based on its relation to other device process parameters and their physical dependencies.

The DC characteristics are obtained by simulations with the AMS CMOS 0.35 μm model in CADENCE. The device used is NMOS with channel width and length of 10 μm and 315 μm respectively. The simulated characteristics for the extraction process are:

- output characteristic Id (Vds) @ Vgs, and
- transfer characteristic Id (Vgs) @ Vbs.

The received simulation data is transferred to the Extract CAD software as a text file.

The flowchart on Figure 1 depicts a step-by-step guideline for software usage.

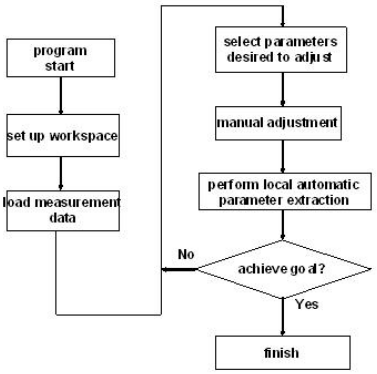

Figure 1. Workflow chart of Extract CAD tool.

On Figure 2 DC characteristics in text format and waveforms from CADENCE are illustrated. The text file is fed as an input for the extraction program.

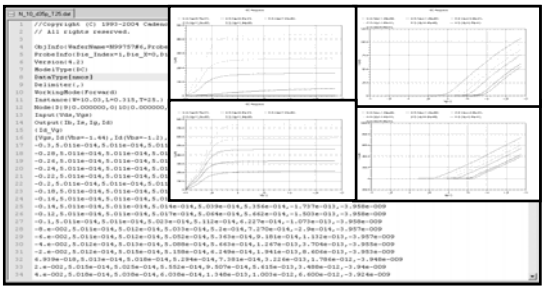

Figure 2. DC characteristics in text format.

In order to begin optimization process accurate values for process parameters are required. After calculation of the parameter values they are input in the extraction tool for further tuning purposes. The program window is given on Figure 3.

An important step is to choose the parameters which will be used in the process of optimization. The PSP 102.1 model has 70 such parameters. If all the parameters are used in optimization process this may result in lack of convergence. To ensure convergence we choose only the parameters with most significant influence on the characteristics. This is determined experimentally. The parameters that are to be fitted are given in Table 2.

A comparison of the optimization results is given on Figure 4.

TABLE 2. PART OF THE MODEL PARAMETERS FITTED.

Name	Unit	Default	Min	Max	Description
Process Parameters					
VFB	V	-1	-	-	Flat-band voltage at TR
TOX	m	$7.6\cdot10^{-9}$	10^{-10}	-	Gate oxide thickness
NEFF	m^{-3}	$2.12\cdot10^{+23}$	10^{+20}	10^{+26}	Substrate doping
NP	m^{-3}	586	0	-	Gate poly-silicon doping
TOXOV	m	$7.6\cdot10^{-9}$	10^{-10}	-	Overlap oxide thickness
CT	-	0	0	-	Interface states factor
NOV	m^{-3}	$5\cdot10^{+25}$	10^{+20}	10^{+27}	Effective doping for overlap region
DPHIB	V	0	-	-	Offset of Phi_beta
DNSUB	V^{-1}	0	0	1	Effective doping bias-dependence parameter
NSLP	V	0.05	10^{-3}	-	Effective doping bias-dependence parameter
VNSUB	V	0	-	-	Effective doping bias-dependence parameter
DIBL Parameters					
CF	V^{-1}	0	0	-	DIBL parameter
CFB	V^{-1}	0	0	1	Back-bias dependence of CF
Mobility Parameters					
BETN	$m^2/V/s$	$7\cdot10^{-2}$	0	-	Product of channel aspect ratio and Zero field mobility at TR
MUE	m/V	0.5	0	-	Mobility reduction coefficient at TR
THEMU	-	1.5	0	-	Mobility reduction coefficient at TR
CS	-	0	0	-	Coulomb scattering parameter at TR
XCOR	V^{-1}	0	0	-	Non-universality parameter
FETA	-	1	0	-	Effective field parameter
Channel Length Modulation (CLM) Parameters					
ALP	-	0.01	0	-	CLM pre-factor
ALP1	V	0	0	-	CLM enhancement factor above threshold
ALP2	V^{-1}	0	0	-	CLM enhancement factor below threshold
VP	V	0.05	10^{-10}	-	CLM logarithmic dependence parameter
Velocity Saturation Parameters					
THESAT	V^{-1}	1	0	-	Velocity Saturation Parameter at TR
THESATB	V^{-1}	0	-0.5	1	Back-bias dependence of velocity saturation
THESATG	V^{-1}	0	-0.5	-	Gate-bias dependence of velocity saturation
Saturation Voltage Parameter					
AX	-	3	2	-	Linear/saturation transition factor

For each parameter the minimum and maximum values has to be specified. This again is done according to the influence of each parameter to the characteristic curves. Some of these values are directly taken from the PSP model documentation as given parameter limitation.

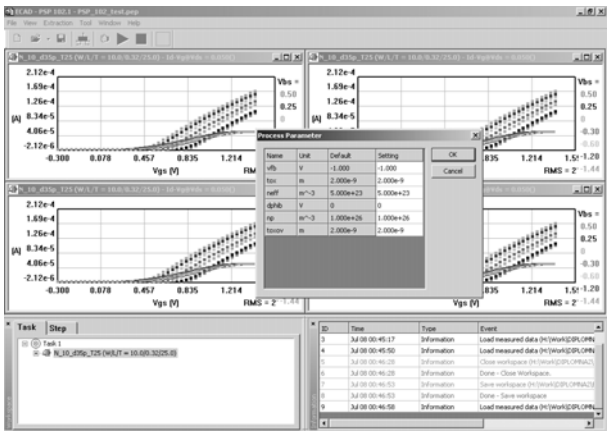

Figure 3. DC characteristics visualization in Extract CAD and window to enter the new process parameters

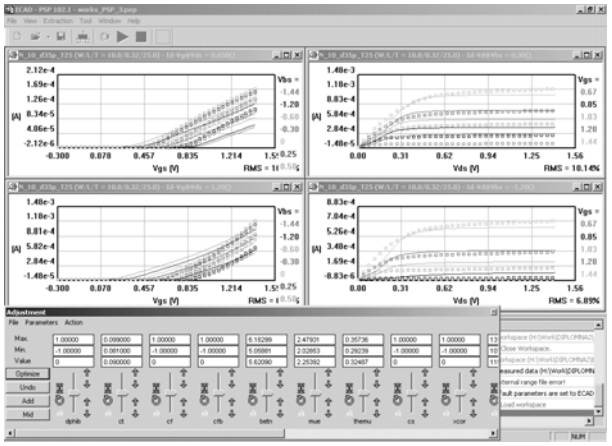

Figure 4. Optimization results.

The program allows optimization to be made manually or automatically. When done automatically the program tries to minimize the range for each parameter according to the specification. The process is iterative and some times takes a long time to complete. When the error is minimized the model card could be extracted.

These values are then used in the PSP Verilog-A model.

III. SIMULATIONS

Simulations of the output transistor characteristics from the specific design kit library are given on Figure 5.

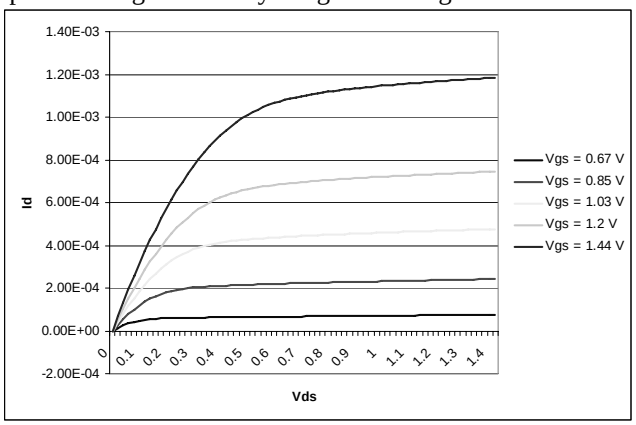

Figure 5. Output characteristics of the transistor from the technology library.

On Figure 6 the simulations of the output characteristic for Verilog-A model are presented.

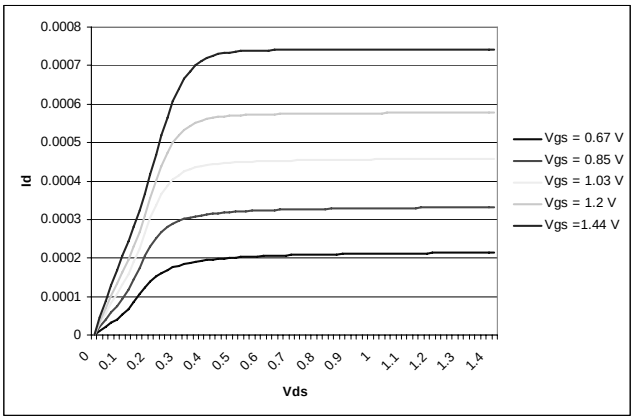

Figure 6. Output characteristics for Verilog-A model.

On figures 7 and 8 the simulation results of the transfer characteristics for transistor from the technology and the Verilog-A model are presented, respectively.

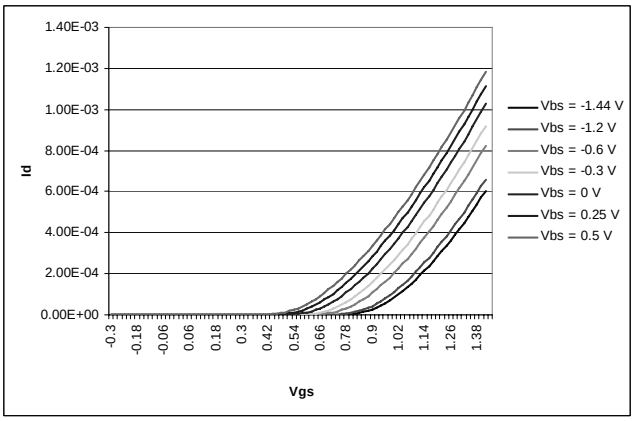

Figure 7. Transfer characteristics of the transistor from the technology library.

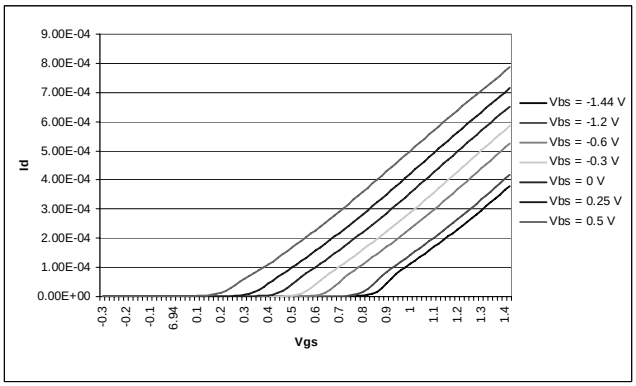

Figure 8. Transfer characteristics for Verilog-A model.

IV. CONCLUSIONS

A method for adaptation of the PSP Verilog-A code in CADENCE is suggested. A mechanism for extraction of the model parameters for a specific technology is presented. Extraction is aided by the Extract CAD tool. The process parameters that are not explicitly given in the technology specifications are calculated. Fitting of PSP parameters to technology parameters that are extracted through simulations is produced using the BSIM model of the given technology. Simulation results with the adapted Verilog-A PSP model prove to give acceptable predictions. The proposed method gives an opportunity for further finetuning of the predictions accuracy.

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